FIG. 1

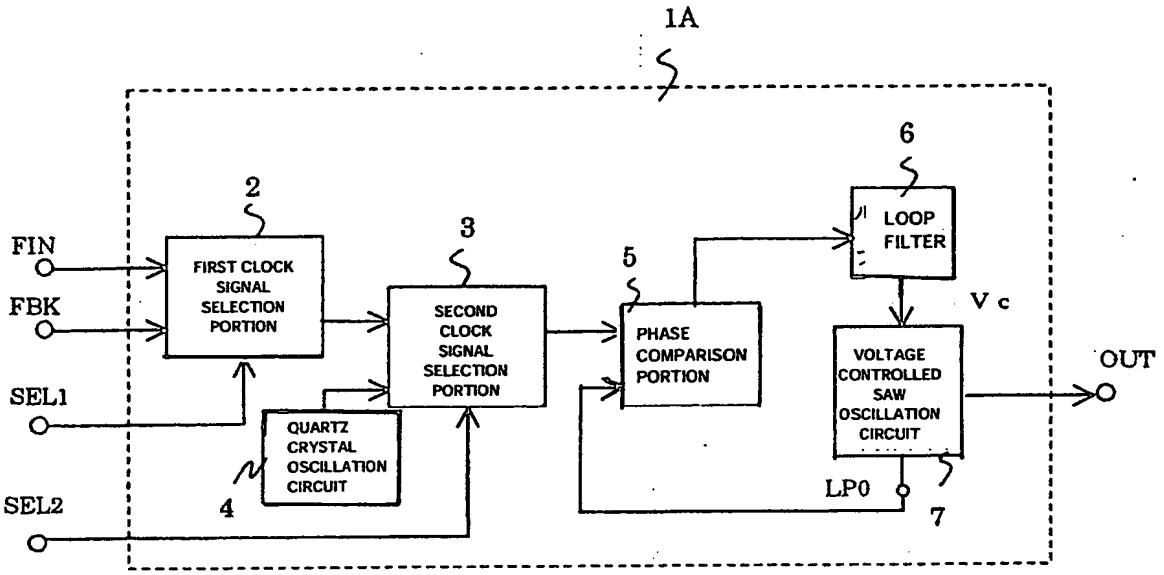

FIG. 2

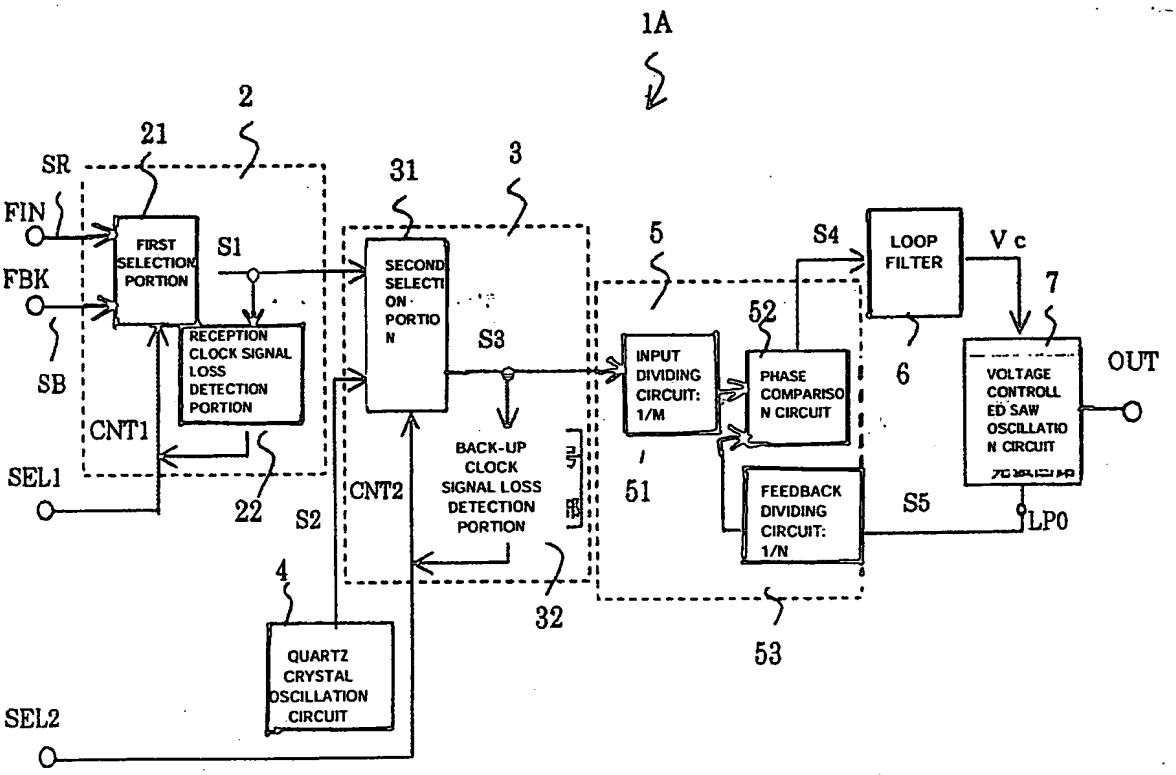

FIG. 3

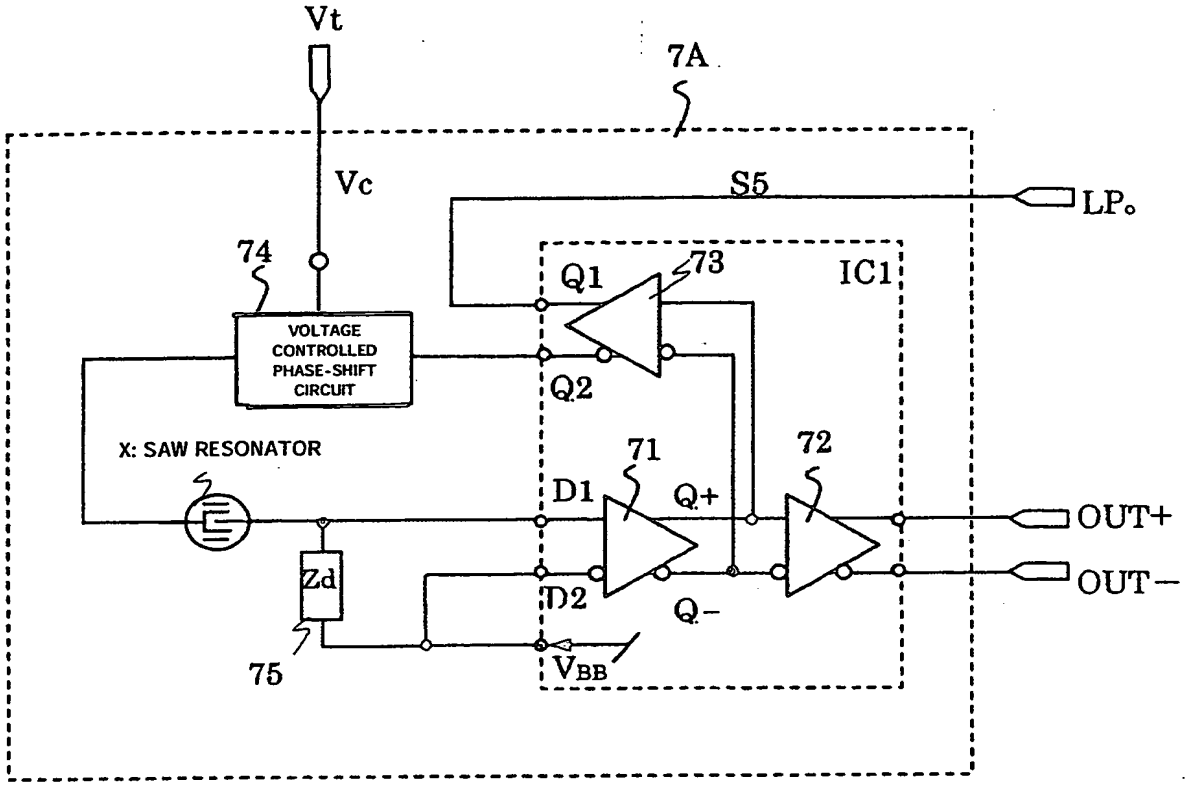
Vt
7A
Vc
S5
LPo
74
Q1
73
IC1
VOLTAGE CONTROLLED PHASE-SHIFT CIRCUIT
Q2
X: SAW RESONATOR
71
72
D1
Q+
OUT+
Zd
D2
Q−
OUT−
75
VBB

FIG. 5

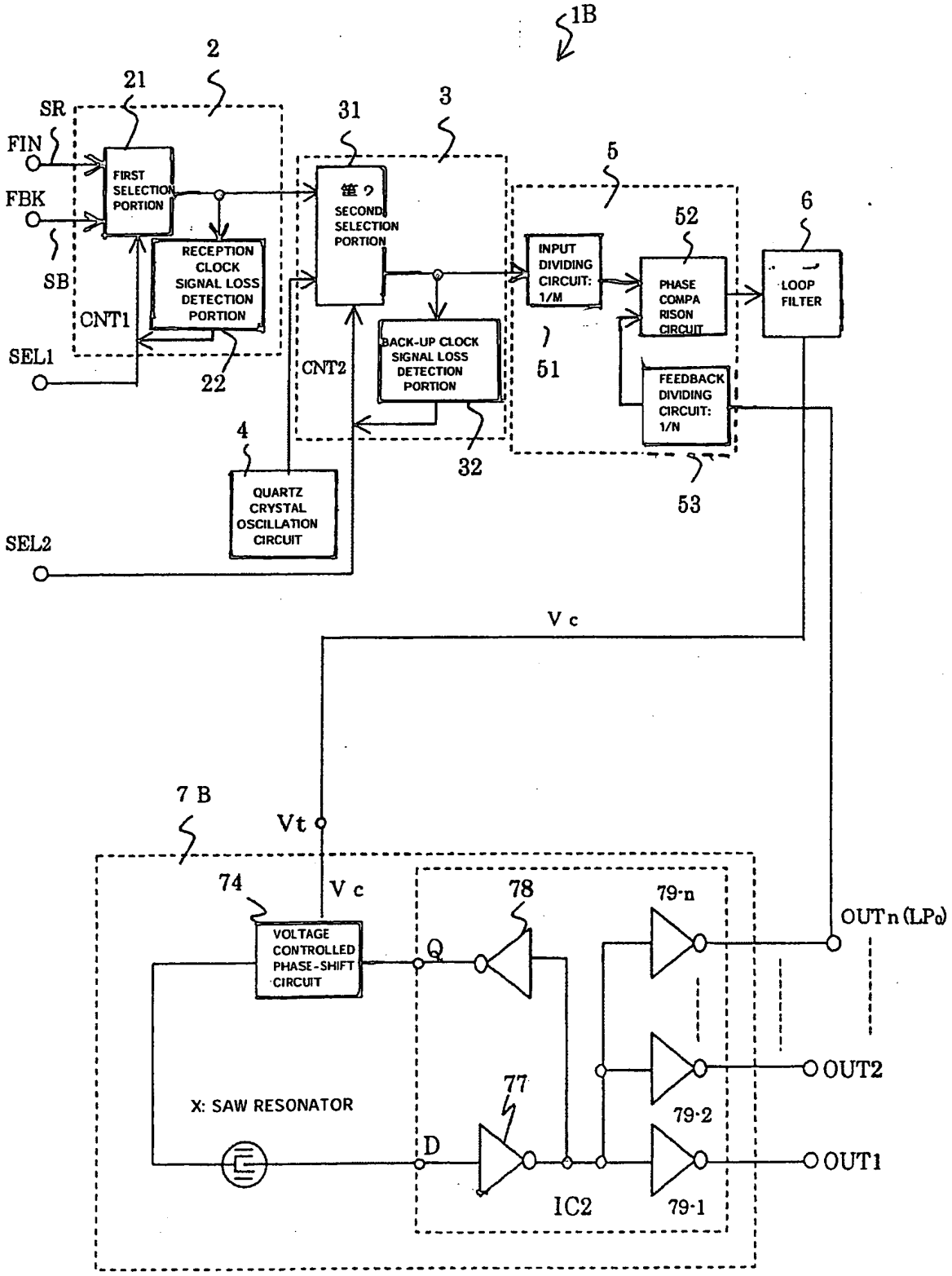
1B
2
21
SR
FIN
FBK
SB
FIRST SELECTION PORTION
RECEPTION CLOCK SIGNAL LOSS DETECTION PORTION
CNT1
SEL1
22
3
31
SECOND SELECTION PORTION
CNT2
BACK-UP CLOCK SIGNAL LOSS DETECTION PORTION
32
4
QUARTZ CRYSTAL OSCILLATION CIRCUIT
SEL2
5
INPUT DIVIDING CIRCUIT: 1/M
51
52
PHASE COMPARISON CIRCUIT
FEEDBACK DIVIDING CIRCUIT: 1/N
53
6
LOOP FILTER
Vc
7B
Vt
74
Vc
VOLTAGE CONTROLLED PHASE-SHIFT CIRCUIT
X: SAW RESONATOR
Q
78
D
77
IC2
79-n
79-2
79-1
OUTn (LPo)
OUT2
OUT1

FIG. 6

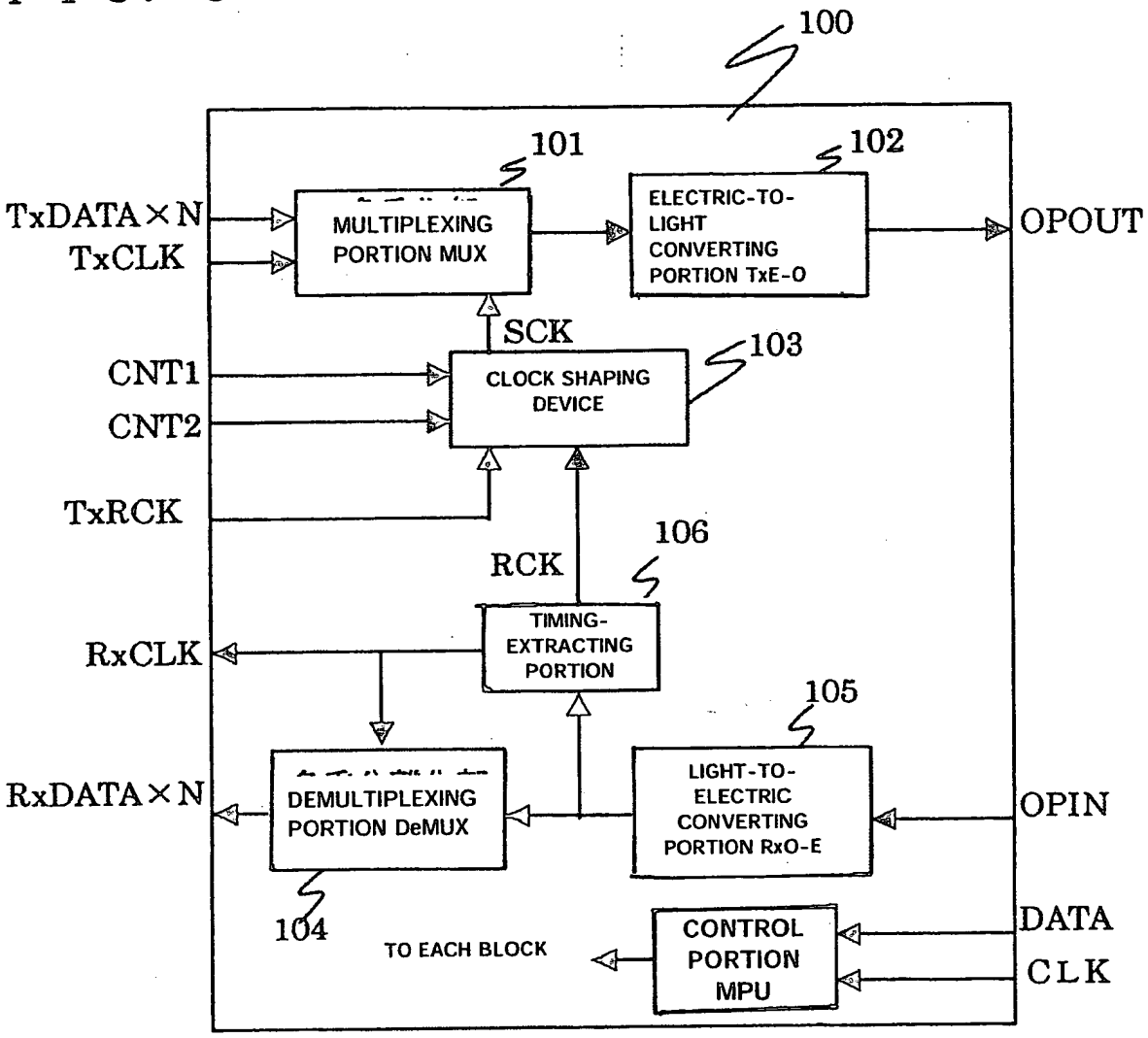
100
101
102
TxDATA×N
TxCLK
MULTIPLEXING PORTION MUX
ELECTRIC-TO-LIGHT CONVERTING PORTION TxE-O
OPOUT
SCK
CNT1
CNT2
CLOCK SHAPING DEVICE
103
TxRCK
RCK
106
TIMING-EXTRACTING PORTION
RxCLK
105
RxDATA×N
DEMULTIPLEXING PORTION DeMUX
LIGHT-TO-ELECTRIC CONVERTING PORTION RxO-E
OPIN
104
TO EACH BLOCK
CONTROL PORTION MPU
DATA
CLK

FIG. 7
Prior Art

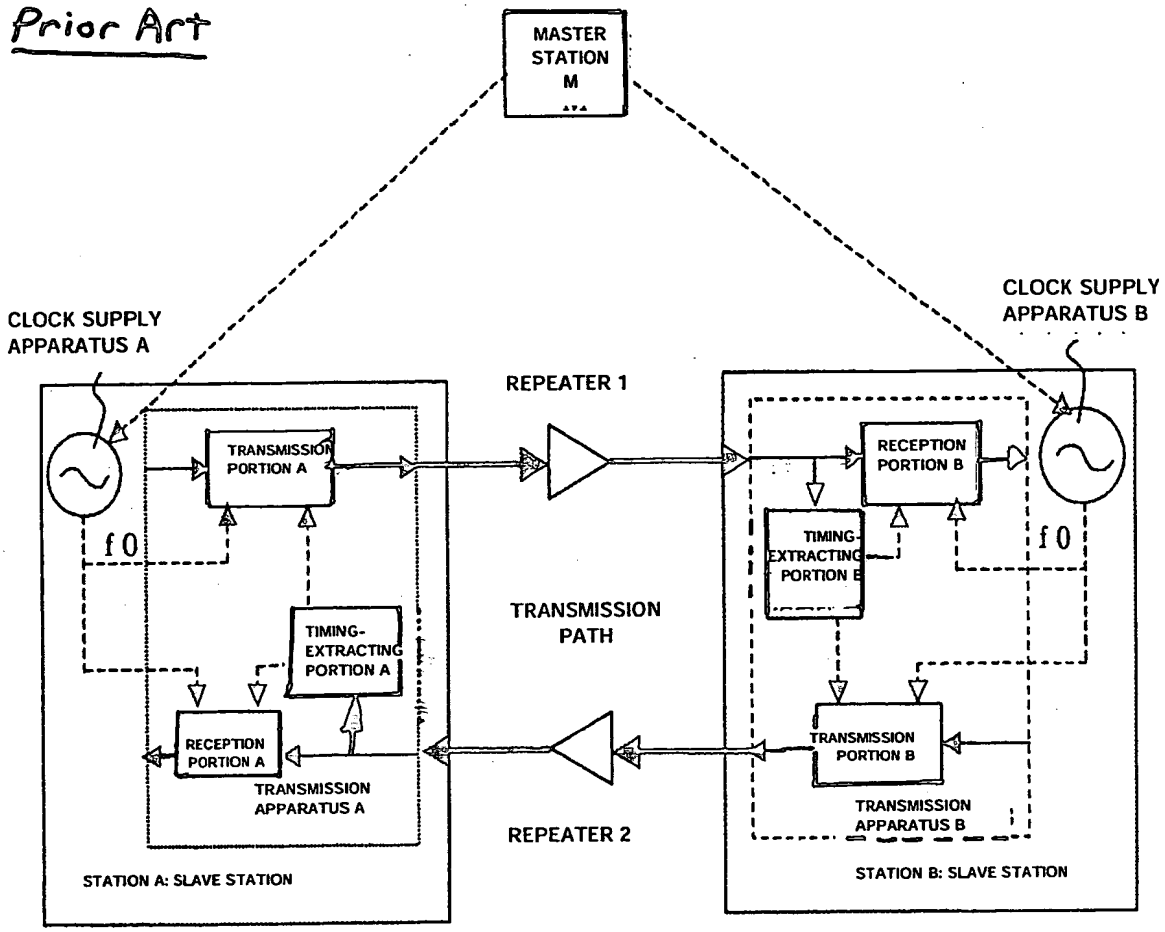

FIG. 8
Prior Art

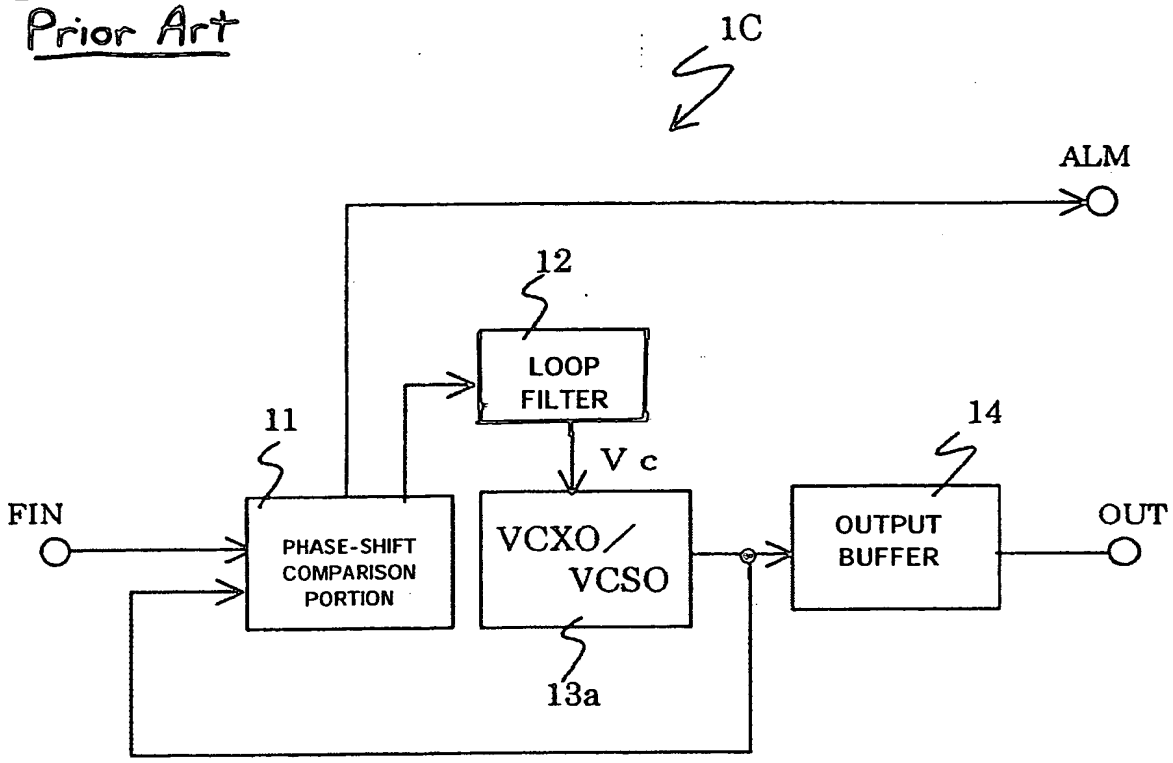

FIG. 9
Prior Art

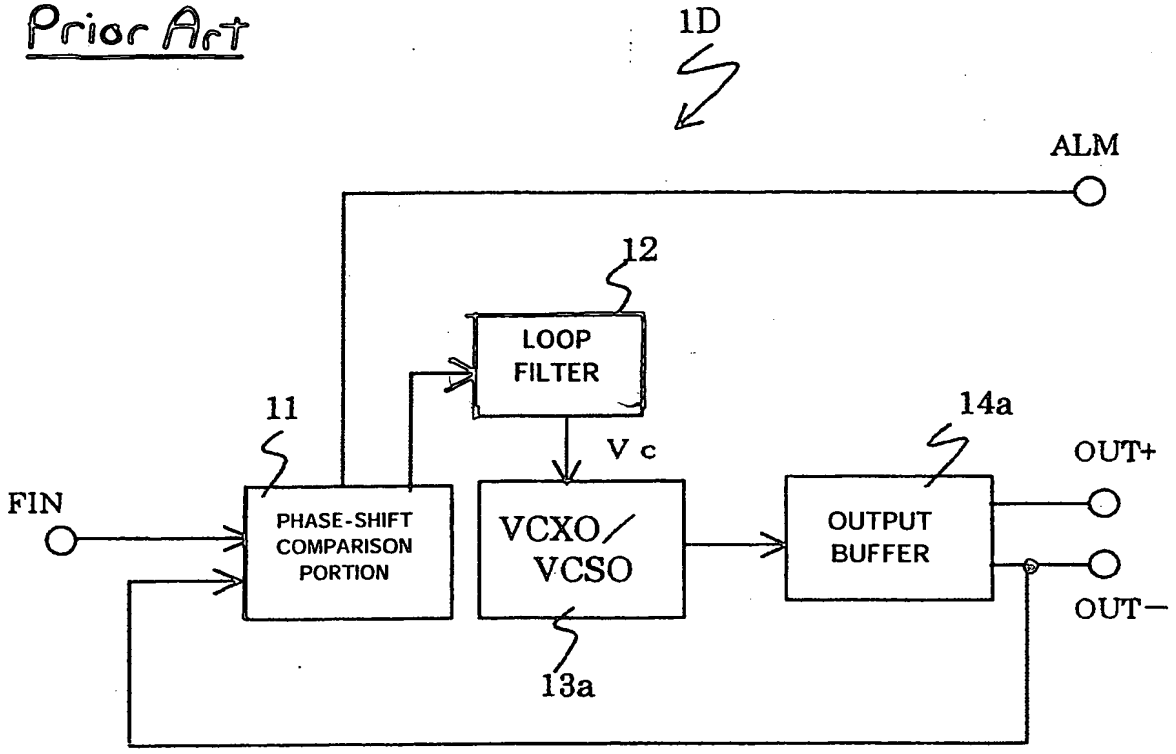

FIG. 10
Prior Art